

LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor package comprising:
a semiconductor die having a control electrode and a first power electrode on a first major surface thereof, and a second power electrode on a second major surface thereof opposite the first major surface opposite surfaces;
a lead frame including a control lead, and a strap portion electrically connected to the first power electrode and terminating at a first power lead lying in a plane and having a strap cupped out of the plane of the lead frame to provide a nest, which is sized to receive the silicon die, an inner surface of the strap being in electric contact with one of the opposite surfaces of the semiconductor die received in the nest of the lead frame; and
a molded housing, wherein the control lead and the first power lead are coplanar and are exposed through a major surface of the molded housing, and wherein the second power electrode is electrically connected through the major surface of the molded housing molded over and protecting the lead frame and the silicon die; the other surface of the semiconductor die being exposed for surface mounting connection with a support surface.
2. (Original) The semiconductor package defined in claim 1, wherein the lead frame extends along a longitudinal axis and has two laterally spaced rails bridged by the strap.
3. (Original) The semiconductor package defined in claim 1, wherein the semiconductor die is a MOSFET whose one surface has a source electrode attached to the inner surface of the strap, and the other surface of the silicon die has a drain electrode attachable to a printed circuit board.
4. (Cancelled)
5. (Cancelled)

6. (Original) The semiconductor package defined in claim 3, further comprising solder bumps, which are distributed across either the top side electrode or the inner surface of the strap, for soldering the source electrode to the strap.

7. (Original) The semiconductor package defined in claim 3, further comprising conductive epoxy between the source electrode and the inner surface of the strap to provide electric contact therebetween.

8. (Original) The semiconductor package defined in claim 3, further comprising a polyamide tape having adhesive opposite surfaces which are attached to the source electrode and to the inner surface of the strap, respectively.

9. (Cancelled)

10. (Cancelled)

11. (Original) The semiconductor package device defined in claim 1, further comprising an least one other strap displaced out of the plane of the lead frame.

12. (Original) The semiconductor package device defined in claim 1, wherein the other surface of the semiconductor die extends so that it at least terminates in the same plane as a bottom surface of the housing.

13. (Currently Amended) A lead frame for a semiconductor die, the lead frame lying in a plane and having a plurality of coplanar sides, which define a nest sized to receive the semiconductor die, and a strap displaced out of the plane of the lead frame and extending across the nest to bridge two coplanar sides for positioning the semiconductor die in the nest so that a bottom surface of the semiconductor die, which faces away from the strap, is exposed for surface mounting connection; wherein the coplanar sides of the lead frame have respective bottom

surfaces which are coplanar with the bottom surface of the semiconductor die; further having a housing molded over and protecting the lead frame and the semiconductor die; the bottom surfaces of the coplanar sides and of the semiconductor die being flush with or extend beyond a bottom surface of the housing.

14. (Cancelled)

15. (Cancelled)

16. (Original) A method for manufacturing a semiconductor package comprising the steps of:

providing an elongated lead frame lying in a plane;

cupping a strap from the plane of the lead frame, thereby providing a nest in the lead frame;

inserting a semiconductor die in the nest so that a bottom surface of the semiconductor die is exposed for surface mounting connection; and

establishing electric contact between a top surface of the semiconductor die and an inner surface of the cupped strap.

17. (Original) The method defined in claim 16, further comprising the step of overmolding the lead frame with the semiconductor die with a plastic mold, thereby providing a housing which protects the lead frame and the semiconductor die.

18. (Original) The method defined in claim 16, wherein the semiconductor die is MOSFET whose top surface is the source electrode, the method further comprising the steps of attaching the top surface of the MOSFET to the inner surface of the cupped strap, and inverting the lead frame to provide a wire bond on the lead frame between the gate electrode of the MOSFET and a protrusion formed on the lead frame and extending into the nest after the

semiconductor die has been mounted to the lead frame but before the overmolding of the lead frame.

19. (Original) The method defined in claim 17, further comprising the step of deflashing the molded lead frame.

20. (Original) The method defined in claim 17, further comprising the step of singulating the molded lead frame to form a plurality of frame segments each having a respective cupped strap and a respective semiconductor device, thereby producing a multiplicity of individual semiconductor packages.

21. (New) A semiconductor package comprising:

a semiconductor die including a first power terminal disposed on a first major surface thereof and a second power terminal disposed on a second major surface thereof;

a conductive strap including a first portion electrically connected to said first power terminal and extending between at least said first power terminal and said second power terminal and terminating at a first external power lead;

a molded housing in which said die is disposed, and including a common major surface opposite said first major surface of said die; wherein said first external power lead is exposed through said common major surface, and said second power terminal is electrically connectable through said common major surface.

22. (New) A semiconductor package according to claim 21, wherein said die includes a control terminal, and further comprising a control lead electrically connected to a control terminal, said control lead being exposed through said common major surface of said molded housing.

23. (New) A semiconductor package according to claim 22, wherein said control terminal is electrically connected to said control lead by a wire bond.

24. (New) A semiconductor package according to claim 21, wherein said second power terminal and said first external power lead are coplanar.

25. (New) A semiconductor package according to claim 21, wherein said conductive strap includes a second portion connected to said first portion and extending between at least said first power terminal and said second power terminal and terminating at a second external power lead.

26. (New) A semiconductor package according to claim 25, wherein said second external power lead is disposed on a side of said die opposite said first external power lead, whereby said strap is formed in a shape of a cup.

27. (New) A semiconductor package according to claim 21, wherein said die is a MOSFET in which said first power terminal is a source terminal and said second power terminal is a drain terminal.

28. (New) A semiconductor package according to claim 27, wherein said die further includes a gate terminal electrically connected to an external gate lead by a wire bond, said external gate lead being exposed through said common major surface of said molded housing.